Amendments to the Specification:

Please replace the paragraph beginning on page 4, line 5 with the following:

Fig. 5 illustrates an embodiment with a RAM associated with the flash NAND device.

Fig. [[5]]6 illustrates a representative timing diagram for address and communication lines provided between the central process unit and serial memory device.

Please replace the paragraph beginning on page 8, line 15 with the following:

In accordance with the subject system, in the event that code sequence are forced to utilize loops, jumps, conditional jumps, or the like, a boot program may suitably copy itself into associated RAM 54 as illustrated in Fig. 5. Such a copy function is provided itself from sequentially executing instructions. After completion of such a copying operation, the boot program may transfer execution to that portion of the program which has been copied into an associated RAM. As illustrated in Fig. 5, MPU 50 is coupled to NAND 52. The boot program is copied on I/O lines 56 from NAND 52 to RAM 54. RAM 54 is addressable by MPU 50 using address lines 58.

Please replace the paragraph beginning on page 6, line 5 with the following:

The sequence noted above is suitably activated by a dedicated chip enable to signal CE[[2]]# which is suitably assertive on a memory device or power-on reset detection circuitry by a reset pin, such as that illustrated by ~~RST~~CS#. Such signals suitably generates an internal signal within the memory device 12 to enable the afore-described sequence mode. As will be apparent from a review of Fig. 1, the address lines 16 are not used in a conventional sense as would be with an addressing scheme in a random access memory device.

Please replace the paragraph beginning on pag 7, line 15 with the following:

The sequence mode noted above includes two functions. A first function is to enable serial data output from a memory device. This is suitably accomplished by toggling the output enable OE#, or a similar signal, such as the read enable RE#, of an associated microprocessor. In the preferred embodiment, the data represents sequential microprocessor instructions and thus no address pins are required. When a sequence is enabled, the memory device in the preferred embodiment automatically loads its internal register from an associated memory cell area which

holds initial boot strap code as is illustrated in Fig. 4. As illustrated therein, a memory cell 40 includes a boot strap program area 42 which is selectively placed in data communication with a register 44. A memory cell area 40 is suitably a primary memory cell or alternatively isolated from a primary cell memory area, such as a redundant memory cell array. The register area [[42]]44 provides for addressing within the memory cell 40. It is to be appreciated that even the designated internal register 44 may be used to store data. When used in a boot sequence, a boot strap code size may vary from one page length, in the case of NAND flash memory to more than one page length by use of sequential read functions, or other analogous functions such as gapless sequential read functions typically provided with NAND flash memory devices as will be appreciated by one of ordinary skill in the art. It will therefore be appreciated that an initial boot strap sequence can be any suitable length as may be required for a particular application.

Please replace the paragraph beginning on page 8, line 20 with the following:

Turning now to Fig. [[5]]6, a suitable timing diagram for address lines, chips lines, output enable lines and data lines, as illustrated in the foregoing figures, is described. With the relative timing as illustrated in Fig. [[5]]6, it would be appreciated that memory such as NAND flash devices which do not possess address pins may be directly tied to a processor bus which has typical bus timing as illustrated by the figure. Thus, the system provides for use of boot memory without address pins and is particularly advantageous for allowing for a boot sequence to be completed from a NAND memory device.